What is claimed is:

1. A data modulation method comprising:

multiplexing input data according to multiplexing information;

inserting a synchronization codeword including the multiplexing information for a multiplexed data stream, and performing data modulation and outputting plural modulated data streams; and

selecting a respective one of the modulated data streams having a DC component which is smallest from among the plural modulated data streams.

2. The method of claim 1, further comprising:

determining the multiplexing information to multiplex the input data according to whether a parity of the synchronization codeword, which is a number of bits having a value of 1, is even or is odd.

3. The method of claim 2, further comprising: changing a parity control bit to 0 or 1 to control of the parity of the synchronization codeword.

4. The method of claim 2, wherein the synchronization codeword comprises a synchronization body and a multiplexing ID to control the parity.

5. The method of claim 2, wherein the synchronization codeword comprises a synchronization body, a synchronization ID, and a multiplexing ID to control the parity.

6. The method of claim 2, wherein the synchronization codeword comprises a synchronization body and a synchronization ID mixed in with a multiplexing ID to control the parity.

7. A data modulation method, according to which m-bit source data is converted into an n-bit codeword where $n \geq m$ and a minimum constraint length is d and a maximum constraint length is k, the method comprising:

multiplexing input data segmented by a predetermined length according to multiplexing information by discontinuously scrambling the segmented input data;

inserting a synchronization codeword including the multiplexing information for a multiplexed data stream, and performing run length limited modulation and outputting plural modulated data streams; and

selecting a respective one of the modulated data streams having a DC component which is smallest from among the modulated data streams.

8. The method of claim 7, further comprising:

determining the multiplexing information to multiplex the input data according to whether a parity of the synchronization codeword, which is a number of bits having a value of 1, is even or is odd.

9. The method of claim 8, further comprising:

changing a parity control bit to 0 or 1 to control of the parity of the synchronization codeword.

10. The method of claim 8, wherein the synchronization codeword comprises a synchronization body, which has a predetermined pattern having a maximum run length violating a maximum constraint length k condition, and a multiplexing ID to control the parity.

11. The method of claim 8, wherein the synchronization codeword comprises a synchronization body, which has a predetermined pattern having a maximum run length violating a maximum constraint length k condition, a synchronization ID, and a multiplexing ID to control the parity.

12. The method of claim 8, wherein the synchronization codeword comprises a synchronization body, which has a predetermined pattern having a maximum run length violating a maximum constraint length k condition, and a synchronization ID mixed in with a multiplexing ID to control the parity.

13. The method of claim 8, wherein the multiplexing of the input data comprises:

generating first converted data from the input data by performing an exclusive OR operation on initial 1-bit multiplexing information and immediately subsequent m-bit data as a first code modulation unit for two types of multiplexed data rows;

outputting 2^{nd} through $(q-1)^{th}$ code modulation units without performing any exclusive OR operation, where q is a scramble spacing index;

generating next converted data from the input data by performing another exclusive OR operation on the first converted data of the first code modulation unit and data of a qth code modulation unit; and

repeatedly performing further exclusive OR operations every qth code modulation unit up to a final code modulation unit of the input data row.

14. The method of claim 8, wherein in the performing of the run length limited modulation, a weak DC-free run length limited modulation, which is DC free but has insufficient DC suppression performance, is performed.

15. A data modulation apparatus comprising:

a multiplexer which multiplexes input data according to multiplexing information;

a modulator which inserts a synchronization codeword including the multiplexing information into the multiplexed input data for a multiplexed data stream, and performs modulation and outputs plural modulated data streams; and

a selector which selects a respective one of the modulated data streams having a DC component which is smallest from among the plural modulated data streams.

16. The apparatus of claim 15, further comprising:

determining the multiplexing information to multiplex the input data according to whether a parity of the synchronization codeword, which is a number of bits having a value of 1, is even or is odd.

17. The apparatus of claim 15, further comprising:

changing a parity control bit to 0 or 1 to control of the parity of the synchronization codeword.

18. The apparatus of claim 15, wherein the synchronization codeword comprises a synchronization body and a multiplexing ID to control the parity.

19. The apparatus of claim 15, wherein the synchronization codeword comprises a synchronization body, a synchronization ID, and a multiplexing ID to control the parity.

20. The apparatus of claim 15, wherein the synchronization codeword comprises a synchronization body and a synchronization ID mixed in with a multiplexing ID to control the parity.

21. A data modulation apparatus, which converts m-bit source data into an n-bit codeword where $n \geq m$ and a minimum constraint length is d and a maximum constraint length is k, the apparatus comprising:

a pseudo scramble multiplexer which multiplexes input data segmented by a predetermined length according to multiplexing information by discontinuously scrambling the segmented input data;

a modulator which inserts a synchronization codeword including the multiplexing information into the multiplexed input data for a multiplexed data stream, and performs run length limited modulation and outputs plural modulated data streams; and

a selector which selects a respective one of the modulated data streams having a DC component which is smallest from among the modulated streams.

22. The apparatus of claim 21, further comprising: determining the multiplexing information to multiplex the input data according to whether a parity of the synchronization codeword, which is a number of bits having a value of 1, is even or is odd.

23. The apparatus of claim 22, further comprising: changing a parity control bit to 0 or 1 to control of the parity of the synchronization codeword.

24. The apparatus of claim 22, wherein the synchronization codeword comprises a synchronization body, which has a predetermined pattern having a maximum run length violating a maximum constraint length k condition, and a multiplexing ID to control the parity.

25. The apparatus of claim 22, wherein the synchronization codeword comprises a synchronization body, which has a predetermined pattern having a maximum run length violating a maximum constraint length k condition, a synchronization ID, and a multiplexing ID to control the parity.

26. The apparatus of claim 22, wherein the synchronization codeword comprises a synchronization body, which has a predetermined pattern having a maximum run length violating a maximum constraint length k condition, and a synchronization ID mixed in with a multiplexing ID to control the parity.

27. The apparatus of claim 22, wherein the pseudo scramble multiplexer comprises an exclusive OR gate disposed every qth, where q is scramble spacing index, and generates first converted data from the input data by performing an exclusive OR operation on initial 1-bit multiplexing information and immediately subsequent m-bit data as a first code modulation unit for two types of multiplexed data rows, outputs 2^{nd} through $(q-1)^{th}$ code modulation units without performing any exclusive OR operation, generates next converted data from the input data by performing another exclusive OR operation on the first converted data of the first code modulation unit and data of a qth code modulation unit, and repeatedly performs further exclusive OR operations every qth code modulation unit up to a final code modulation unit of the input data row.

28. The apparatus of claim 22, wherein the modulator comprises:

first and second synchronization codeword inserters, which insert the synchronization codeword including the multiplexing information, for two types of multiplexed data streams; and

first and second DC-free run length limited encoders, which perform a weak DC-free run length limited modulation that is DC free but has insufficient DC suppression performance on the two types of multiplexed data streams.

29. The apparatus of claim 28, wherein the first and second DC free run length limited encoders, which do not use a DC suppression control conversion table having an additional bit, generate codewords suited to predetermined constraint length conditions, group the codewords according to the predetermined constraint length conditions, and perform the run length limited modulation using a main code conversion table containing the codewords so that a code row of a source word has a DC control operation, and a DC suppression control sub-conversion table for codewords which satisfy the predetermined constraint length conditions and are not required in the main code conversion table.

30. A data modulation method comprising:

multiplexing input data according to parity data of a synchronization codeword;

inserting the synchronization codeword including the parity data for the multiplexed input data to produce a multiplexed data stream;

performing data modulation on the multiplexed data stream having the synchronization codeword inserted to output plural modulated data streams; and

selecting and outputting a respective one of the modulated data streams having a DC component which is smallest from among the plural modulated data streams.

31. A data modulation method, according to which m-bit source data is converted into an n-bit codeword where $n \geq m$ and a minimum constraint length is d and a maximum constraint length is k, the method comprising:

multiplexing input data segmented by a specified length according to parity data of a synchronization codeword by intermittently rearranging the segmented input data to produce a multiplexed data stream;

inserting the synchronization codeword including the parity data for the multiplexed data stream;

performing run length limited modulation on the multiplexed data stream having the synchronization codeword inserted to output plural modulated data streams; and

selecting and outputting a respective one of the modulated data streams having a DC component which is smallest from among the modulated data streams.

32. A data modulation apparatus comprising:

a multiplexer to multiplex input data according to parity data of a synchronization codeword to produce a multiplexed data stream;

a modulator to insert the synchronization codeword including the parity data for the multiplexed data stream, to perform modulation on the multiplexed input data stream having the synchronization codeword inserted, and to output plural modulated data streams; and

a selector to select and to output a respective one of the modulated data streams having a DC component which is smallest from among the plural modulated data streams.

33. A data modulation apparatus to convert m-bit source data into an n-bit codeword where $n \geq m$ and a minimum constraint length is d and a maximum constraint length is k, the apparatus comprising:

a pseudo scramble multiplexer to multiplex input data segmented by a specified length according to parity data of a synchronization codeword by intermittently rearranging the segmented input data to produce a multiplexed data stream;

a modulator to insert the synchronization codeword including the parity data for the multiplexed data stream, to perform run length limited modulation on the multiplexed data stream having the synchronization codeword inserted, and to output plural modulated data streams; and

a selector to select and to output a respective one of the modulated data streams having a DC component which is smallest from among the modulated streams.